QUARTER-MICRON WSi/Au GATE AlGaAs/InGaAs HJFETs FOR Q-BAND POWER APPLICATIONS

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ABSTRACT

Quarter-micron T-shaped (WSi/plated-Au) gate AlGaAs/InGaAs HJFETs for Q-band power applications are reported. Fmax of 170GHz was achieved for the 100μm gate-width device. Fmax's of 115 and 90GHz were realized for 400 and 800μm gate-width devices, respectively, with 100μm unit gate finger width, by reducing the gate parasitic capacitance and the gate resistance employing Au-plating for the gate metal formation. An output power of 25dBm was obtained with a linear gain of 6.6dB at 40GHz band.

INTRODUCTION

Recently, there has been considerable interest in the power performance of pseudomorphic InGaAs/AlGaAs hetero-junction FETs (HJFETs) operating in the millimeter wave frequency range [1,2,3]. However, these studies have mainly focused on the AlGaAs/InGaAs FETs having Al, Ti/Al or Ti/Pt/Au gate metal similar to the baseline technology of low-noise HJFETs. On the other hand, the study of the HJFETs with WSi gate metal has been severely restricted. We can find only a few articles on WSi gate AlGaAs/InGaAs HJFET discussing the low noise performance[4,5].

In this paper, we will report the power performance of quarter-micron WSi/Au gate AlGaAs/InGaAs HJFETs for millimeter wave (Q-band) applications. Fmax of 90GHz was achieved for 800μm gate-width devices with 100μm unit gate finger width, by reducing the gate resistance employing the Au-plating for the gate metal formation, and by reducing the gate to drain parasitic capacitance. An output power of 25dBm was obtained with a linear gain of 6.6 dB at 40GHz band.

DEVICE DESIGN AND FABRICATION

The devices we used in this work were fabricated on AlGaAs/InGaAs hetero-junction MBE wafers. Our devices had n-(1E17 cm-3)/n(3E18cm-3) AlGaAs top layers to increase the gate breakdown voltage BVgd, because one of the most important points to obtain the high performance power HJFET is to increase the drain breakdown voltage.

Figure 1 shows the schematic cross-sectional view for our developed WSi/Au gate AlGaAs/InGaAs HJFET. Figure 2 shows the cross-sectional SEM view. The active layer isolation implemented by double boron implantation and the recess etching were performed before the gate formation. Our device had an offset gate structure in the wide-recess; the distance of the gate to source-side edge of recess was 0.2μm and to drain-

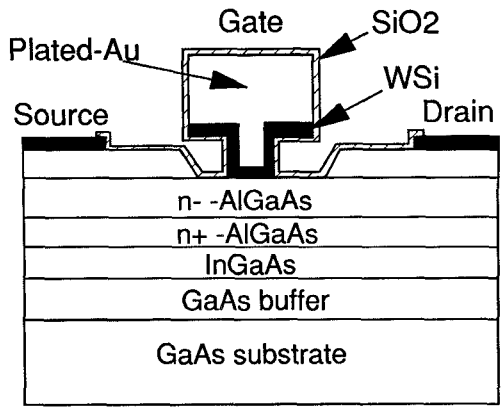

Fig.1 Schematic device structure for WSi/plated-Au gate AlGaAs/InGaAs HJFET

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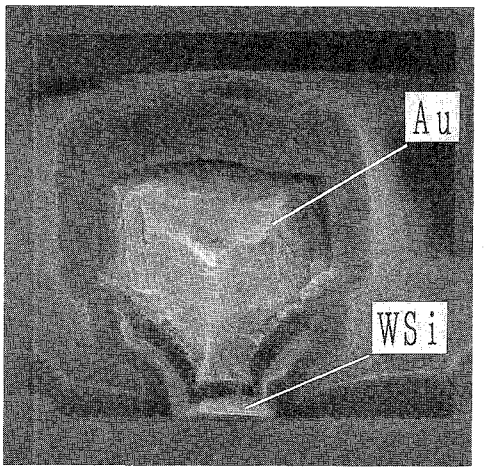

Fig.2 Cross-sectional SEM view of (WSi/Au) gate HJ FET

side edge of recess was 0.3μm. Because the longer the distance from gate to drain-side edge of recess, the higher the fmax.

The quarter micron length gate was successfully formed by 0.45μm photo-lithography technology by employing the silicon dioxide inner side-wall technique. This sub-half micron gate technology without using EB lithography is very important from the productivity point of view. After opening the silicon dioxide where the gate fingers were placed, employing the reactive ion etching technology, we fabricated T-shaped (WSi/TiN/Pt/plated-Au) gates. After WSi sputtering as the Schottky gate metal, the substrate was annealed to remove the damage caused by reactive ion etching and/or WSi sputtering.

In order to form the T-shaped gate, TiN/Pt was sputtered onto the annealed WSi, and photo-resist with 1.0-micron patterning for gold-plating was aligned with the quarter micron gate patterns, and then metals were etched off, employing plated gold as the etching mask. The plated gold layer thickness was about 8000A, and this enables us to obtain the reduced gate resistance. The DC end to end resistance was about 50 ohm/mm compared to 160 ohm/mm for the T-shaped mushroom gate[6]. The gate resistance of the developed device was also nearly one-third of the device having the same structure, except that the gold was sputtered(not plated). The thickness of the sputtered gold was limited to 4000A because the sputtered gold had to be milled off;(not lifted off) and the milling dust had a baneful influence on the FET manufacturing process. This reduced gate resistance resulted in a fmax increase of about 10-20GHz according to our equivalent circuit analysis. Furthermore, this refractory metal multi-layer gate structure is also very reliable and has been successfully employed for our highly reliable micro-wave power MESFETs.

After the T-shaped gate formation, silicon dioxide under the cap was removed and then replaced with a thin silicon dioxide film of 1000A thickness for the final passivation, because the drain-to-gate parasitic capacitance between the cap of the T-shaped gate and the channel layer seriously degrades the fmax of the device. According to our equivalent circuit analysis, the parasitic capacitance can be reduced by nearly 25%(50fF/mm) by removing the dielectric film(SiO2) under the cap, and re-covering with a SiO2 film passivation, resulting in a fmax increase of about 20GHz.

DEVICE PERFORMANCE

We discuss the DC characteristics of the developed quarter micron (WSi/plated Au) gate HJFET. A BVgd (defined at 1mA/mm) of 12V and an Imax of 550mA/mm can be obtained with a transconductance(gm) of 450mS/mm and a threshold voltage of -1.5V. A drain breakdown voltage of over 10 V was also achieved for 1/2Imax condition, which enabled 5V-operation of the device.

Next, microwave characteristics of the developed device are discussed. Figure 3 shows the scattering parameter of the quarter micron (WSi/plated Au) gate HJFET with the 100μm gate width (unit gate finger width was 50μm). The maximum frequency of oscillation (fmax) of the device was 170GHz as shown in figure 4. The fmax's were obtained from the -6dB/octave extrapolation of the maximum unilateral transducer power gain(Gu) calculated from the scattering parameters measured at 4V drain bias voltage.

We measured the S-parameters for the devices varying the unit gate finger width ranging from 25 to 100μm and the number of fingers from 2 to 8. The fmax's derived from the measured S-parameters are shown in figure 5 as functions of the total gate width. Fmax seriously decreased with increase of the total gate width , probably due to the effect of the phase non-uniformity at fingers along the gate bus bar and due to the relatively large series inductance. However the fmax of the devices having 100μm unit gate finger width was higher than the smaller unit finger width devices with the same total gate width. And fmax was 155GHz for the 200μm device, 115GHz for the 400μm device and 90GHz even for the 800μm device with 100μm unit gate width finger at the drain bias voltage of 4V. This remarkable result compared with the results for

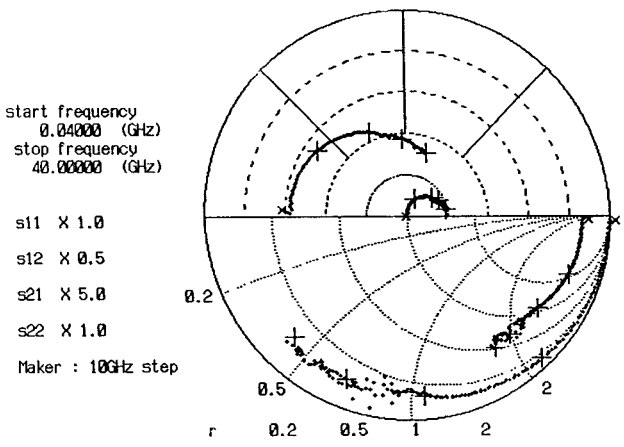

Fig.3 S-parameters of the (WSi/plated-Au) gate AlGaAs/InGaAs HJFET with the total gate width of 100μm

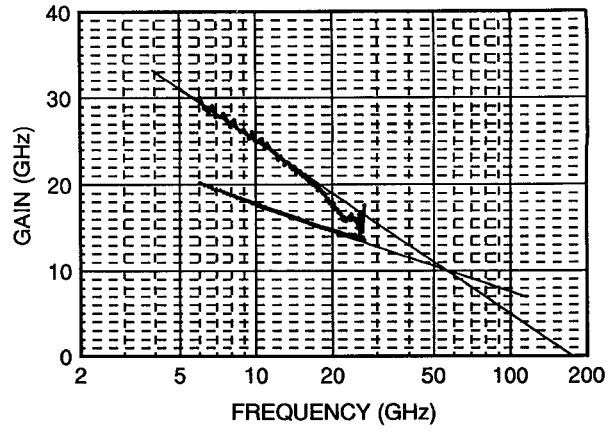

Fig.4 MSG and Gu of the device having the total gate width 100μm as the function of frequency.

devices that employed low-noise baseline technologies (in which the unit gate finger width of the devices for the millimeter-wave applications was 50μm or less[2]), is considered to stem from the low gate resistance, which reduced the gate signal attenuation along the gate finger.

Though the performance of the device having the 150μm unit gate finger width was also examined, fmax was a little bit smaller than the 100μm unit gate width device. Based on these results, the comparatively long unit gate finger width of 100μm was preferred for our device, since it would allow for a smaller chip size for a given total gate width as well as higher linear gain performance. These small-signal performances enabled the devices to be implemented in Q-band power amplifier.

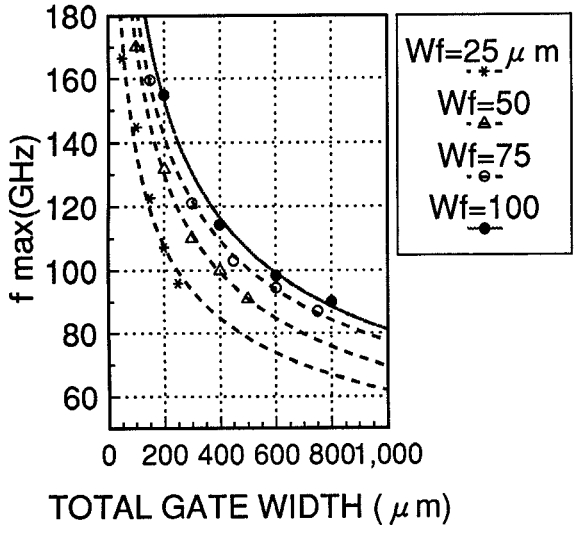

Fig.5 Fmax's of the developed HJFET as functions of the total gate width, ie. varying the unit gate finger width ranging from 25 to 100μm and the number of fingers from 2 to 8.

Microwave power performance was measured at 40GHz band for the devices having the total gate width of 200,400,800μm at the drain bias voltage of 4 and 5V, and the results are summarized in Table 1. An output saturation power (Psat) of 18.5dBm with a linear gain of 9.8dB, and 22dBm with 7.8dB gain was obtained from 200 and 400μm gate width devices, respectively, under the 5V-operation. Figure 6 shows the power and efficiency characteristics of the 800μm gate

tatal gate width (μm)	linear gain at Vds=4/5V (dB)	saturation power at Vds=4/5V (dBm)	efficiency (percent)
200	10.2/9.8	17.2/18.5	-
400	8.2/7.8	20.8/22.0	-
800	7.0/6.6	24.0/25.0	20.0

Table 1 40GHz power performance of quarter-micron (WSi/plated Au) gate InGaAs/AlGaAs HJFET measured at drain bias voltage of 4 and 5V.

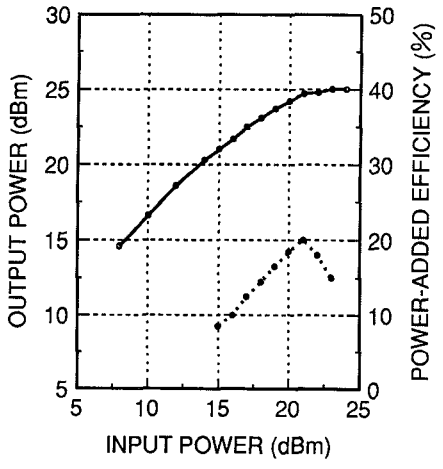

Fig.6 Pin - Pout characteristics at 40GHz band of the quarter-micron (WSi/plated Au) gate HJFET.

width devices. Psat of 25dBm was achieved with 6.6dB linear gain and 4.0dB saturation gain with a 20 percent power added efficiency under the drain bias voltage of 5V.

CONCLUSION

Quarter-micron T-shaped (WSi/plated-Au) gate AlGaAs/InGaAs HJFETs for Q-band power applications are reported for the first time. Fmax of 170GHz was achieved for the 100μm gate width device. And fmax of 115 and 90GHz were realized for 400 and 800μm gate-width devices, respectively, with 100μm unit gate finger width, by reducing the gate parasitic capacitance, and by reducing the gate resistance employing Au- plating for the gate metal formation. An output power of 25dBm was obtained with a linear gain of 6.6dB with 20 percent power added efficiency under 5V-operation. These developed power HJFETs are very practical from the view points of reliability, productivity and the microwave performances.

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